


# APPLICATION DATA SHEET

Electronic Version v14

Stylesheet Version v14.0

<b>Title of Invention</b>	STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SOURCE AND DRAIN REGIONS		
<b>Application Type :</b>		regular, utility	
<b>Attorney Docket Number :</b>		FIS920030199US1	
<b>Correspondence address:</b>			
<b>Customer Number:</b>		032074	
<b>Inventors Information:</b>			
<u>Inventor 1:</u>			
<b>Applicant Authority Type:</b>	Inventor		
<b>Citizenship:</b>	CN		
<b>Given Name:</b>	Huajie		
<b>Family Name:</b>	Chen		
<b>Residence:</b>			
<b>City of Residence:</b>	Danbury		
<b>State of Residence:</b>	CT		
<b>Country of Residence:</b>	US		
<b>Address-1 of Mailing Address:</b>	622 Avalon Lake Road		
<b>Address-2 of Mailing Address:</b>			
<b>City of Mailing Address:</b>	Danbury		
<b>State of Mailing Address:</b>	CT		
<b>Postal Code of Mailing Address:</b>	06810		
<b>Country of Mailing Address:</b>	US		
<b>Phone:</b>			
<b>Fax:</b>			
<b>E-mail:</b>			
<u>Inventor 2:</u>			
<b>Applicant Authority Type:</b>	Inventor		
<b>Citizenship:</b>	US		
<b>Given Name:</b>	Dureseti		
<b>Family Name:</b>	Chidambarrao		

**Residence:**

**City of Residence:** Weston  
**State of Residence:** CT  
**Country of Residence:** US  
**Address-1 of Mailing Address:** 29 Old Mill Road  
**Address-2 of Mailing Address:**  
**City of Mailing Address:** Weston  
**State of Mailing Address:** CT  
**Postal Code of Mailing Address:** 06883  
**Country of Mailing Address:** US  
**Phone:**  
**Fax:**  
**E-mail:**

Inventor 3:

**Applicant Authority Type:** Inventor  
**Citizenship:** RU  
**Given Name:** Oleg  
**Middle Name:** G.  
**Family Name:** Gluschenkov  
**Residence:**  
**City of Residence:** Poughkeepsie  
**State of Residence:** NY  
**Country of Residence:** US  
**Address-1 of Mailing Address:** 160 Academy Street  
**Address-2 of Mailing Address:** Apartment #9H  
**City of Mailing Address:** Poughkeepsie  
**State of Mailing Address:** NY  
**Postal Code of Mailing Address:** 12601  
**Country of Mailing Address:** US  
**Phone:**  
**Fax:**  
**E-mail:**

Inventor 4:

**Applicant Authority Type:** Inventor  
**Citizenship:** BE  
**Given Name:** An  
**Middle Name:** L.  
**Family Name:** Steegen  
**Residence:**  
**City of Residence:** Stamford

**State of Residence:** CT  
**Country of Residence:** US  
**Address-1 of Mailing Address:** 150 Southfield Avenue  
**Address-2 of Mailing Address:** Apartment 2438  
**City of Mailing Address:** Stamford  
**State of Mailing Address:** CT  
**Postal Code of Mailing Address:** 06902  
**Country of Mailing Address:** US  
**Phone:**  
**Fax:**  
**E-mail:**

Inventor 5:

**Applicant Authority Type:** Inventor  
**Citizenship:** CN  
**Given Name:** Haining  
**Middle Name:** S.  
**Family Name:** Yang  
**Residence:**  
**City of Residence:** Wappingers Falls  
**State of Residence:** NY  
**Country of Residence:** US  
**Address-1 of Mailing Address:** 36 Robinson Lane  
**Address-2 of Mailing Address:**  
**City of Mailing Address:** Wappingers Falls  
**State of Mailing Address:** NY  
**Postal Code of Mailing Address:** 12590  
**Country of Mailing Address:** US  
**Phone:**  
**Fax:**  
**E-mail:**

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Assignee 1:

**Organization Name:** International Business Machines Corporation  
**Address-1 of Mailing Address:** New Orchard Road  
**Address-2 of Mailing Address:**  
**City of Mailing Address:** Armonk

**State of Mailing Address:**

NY

**Postal Code of Mailing Address:**

10504

**Country of Mailing Address:**

US

**Phone:**

**Fax:**

**E-mail:**